

The schematic diagram illustrates the proposed system architecture, divided into two main processing units, 301 and 302, and a central control unit 303.

Unit 301: This unit contains a sequence of processing blocks labeled 1 through 4. Block 1 is a feedback loop that receives input from block 4 and feeds it back into block 1. Block 2 is a feedback loop that receives input from block 4 and feeds it back into block 2. Block 3 is a feedback loop that receives input from block 4 and feeds it back into block 3. Block 4 is a feedback loop that receives input from block 4 and feeds it back into block 4. The output of block 4 is fed into block 1.

Unit 302: This unit contains a sequence of processing blocks labeled 1 through 4. Block 1 is a feedback loop that receives input from block 4 and feeds it back into block 1. Block 2 is a feedback loop that receives input from block 4 and feeds it back into block 2. Block 3 is a feedback loop that receives input from block 4 and feeds it back into block 3. Block 4 is a feedback loop that receives input from block 4 and feeds it back into block 4. The output of block 4 is fed into block 1.

Unit 303: This unit contains a large array of processing blocks, numbered 304 through 312. Each block in this array is a feedback loop that receives input from block 4 and feeds it back into block 4. The output of block 4 is fed into block 1.

The diagram shows the interconnections between these units, including data flow and control signals. The system is designed for real-time processing of input signals.

[illegible]

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|----------------------|-----------------------|
| INVESTOR | MASARYKOVA UNIVERZITA |
| GENERÁLNÍ DODAVATEL | |
| MANAŽER PROJEKTU | SYNERGA a.s. |
| GENERÁLNÍ PROJEKTANT | SYNERGA a.s. |
| PRÍMÝ ZPRACOVATEL | SYNERGA a.s. |

TECHNOLOGICKÁ SIT

- BACHY MESTP 1
- BACHY MESTP 2
- KUS
- PŘÍSTUP DOGAVNA PROFESE SLABOTROU
- LIMON
- MODUS
- Mbus

705

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1. IGMP/ICMP ROZVÍZČEČE

2. IGMP/ICMP ROZVÍZČEČE (DELTA CONTROL)

3. 1-REČ JEDNOTKY

4. IGMP/ICMP REČ JEDNOTKY

5. DDP SWITCH

6. ADRESA REČ JEDNOTKY

705

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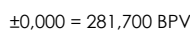
1. ZÁSAHA PRO PŘÍKLONĚNÍ ETHERNETU

2. TERMINATOR

3. PŘEPÍNAČ OCHRANA

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| 01 | |
| 02 | |
| 03 | |

VED. PROJEKTANT ING. DOHNAL RADEK



STAVBA ILBIT

NÁZEV PS - SO D.SO 302.2 - PAVILON A3

NÁZEV VÝKRESU **TOPOLOGICKÉ SCHÉMA MAR**

| | |
|--------|----|
| FORMAT | A4 |
|--------|----|

| STANBA | STUPEN | OSLOPS - SO | CAS | VTURES | REVISE |
|--------|--------|-------------|-----|--------|--------|
| UKB-0 | DPS | D 302.2 | 13 | 008 | 00 |